REMARKS/ARGUMENTS

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on April 18, 2006. This Response incorporates comments and suggestions made during the interview.

Claims 1-25 are pending in the present application. Claims 1, 5-8, 12, 14, 18 and 21-25 are amended. No claims are added and no claims are canceled. Applicants have carefully considered the cited art and the Examiner's comments and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

A new title is provided as required by the Examiner. As discussed during the interview, the provided title is believed to be clearly indicative of the invention to which the claims are directed.

As requested by the Examiner, the paragraph bridging pages 1 and 2 of the specification has been amended to supply the serial numbers of the related applications identified therein.

The Examiner has objected to the terminology in claims 1, 6 and 23. The claims have been amended as requested by the Examiner and are believed to be in proper form. Claims 22 and 25 have also been amended to correct terminology therein and are believed to be in proper form as well.

I. 35 U.S.C. § 101

The Examiner has rejected claims 21-25 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. Applicants respectfully disagree that these claims are directed to non-statutory subject matter; however, to expedite prosecution, the specification has been amended to delete the objectionable subject matter.

Therefore, the rejection of claims 21-25 under 35 U.S.C. § 101 has been overcome.

II. 35 U.S.C. § 102, Anticipation – Claims 1-5 and 8-25

The Examiner has rejected claims 1-5 and 8-25 under 35 U.S.C. § 102(b) as being anticipated by Heisch (U.S. Patent No. 5,774,724). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states as follows:

> As per claim 1, Heisch discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache (Fig. 2 cache 60) in a processor in the data processing system, determining whether an indicator is associated with the instruction (Col. 5 lines 58-65); and forcing an interrupt if the indicator is associated with the instruction (Col. 5 line 66-col. 6 line 6).

Claim 1 of the present application as amended herein is as follows:

> 1. A method in a data processing system for processing instructions, the method comprising:
>
> responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present; and
>
> forcing an interrupt if the performance indicator is present.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Heisch does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Heisch does not teach or suggest "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present"; and "forcing an interrupt if the performance indicator is present".

Heisch is directed to performance monitoring of computer systems. In Heisch, an instruction address breakpoint register (IABR) is provided that stores preselected instruction address breakpoints. The operation of the system in Heisch is described in Col. 5, line 58 to Col. 6, line 13 as follows:

> The basic operation of an IAB is as follows. First, an address of interest may be loaded into the IAB register, whereupon the microprocessor associated with the IABR executes program instructions while the register is monitored. The contents of the IAB register, more specifically, are compared to the address of the particular instruction executing at a given time. This function is shown by the IABR compare block **64** of FIG. 2.
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> At some point when, as a result of this comparison, it is detected that a preselected IAB address is equal to the address of the instruction currently to be executed, the microprocessor will detect this event. The processor will thereby be caused to break out of execution of the current program, whereupon execution will pass to an interrupt handler specifically initialized to handle that breakpoint or exception. This technique is a relatively common one often employed for debugging purposes and the like wherein it is desired to interrupt execution of a program at preselected points for

various reasons. In other words, typically this IAB and associated IABR register allows a programmer to insert an instruction causing the microprocessor to stop operation at a special address and transfer control to another function for purposes of debug, or the like.

As clearly described in the above recitation, as program instructions are executed in Heisch, the IABR is monitored. When a preselected IAB address stored in the IABR matches the address of an instruction currently to be executed, the processor is caused to break out of execution of the current program and pass execution to an interrupt handler. A preselected address stored in the IABR is not a "performance indicator that identifies that execution of the instruction is to be monitored". Heisch merely compares an address stored in the IABR with an address of an instruction to determine if they match. Heisch, therefore, does not disclose "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present", and "forcing an interrupt if the performance indicator is present" as recited in claim 1. Claim 1 as amended, accordingly, is not anticipated by Heisch and patentably distinguishes over Heisch in its present form.

Claims 2-5 depend from and further restrict claim 1 and are also not anticipated by Heisch, at least by virtue of their dependency.

Independent claims 14 and 21 have been amended in a manner similar to claim 1, and are also not anticipated by Heisch for substantially the same reasons as discussed above with respect to claim 1. Claims 15-17 depend from and further restrict claim 14, and claims 22 and 23 depend from and further restrict claim 21 and are also not anticipated by Heisch, at least by virtue of their dependency.

Independent claim 8, as amended herein, is as follows:

8. A method in a data processing system for processing data, the method comprising:

responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present; and

generating an interrupt if the performance indicator is present.

As discussed in detail above, Heisch employs an IABR that stores preselected instruction address breakpoints and causes an interrupt whenever an address of an instruction currently to be executed matches a stored address. Claim 8, on the other hand requires that, responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present". Heisch does not disclose or suggest "responsive to an access of data, determining whether a performance indicator that identifies that access of the data to be monitored is present", and does not anticipate claim 8. Claim 8, accordingly, should also be allowable over Heisch in its present form.

Claims 9-13 depend from and further restrict claim 8 and are also not anticipated by Heisch, at least by virtue of their dependency.

Independent claims 18 and 24 have been amended in a similar manner as claim 8, and are also not anticipated by Heisch for substantially the same reasons as discussed above with respect to claim 8. Claims 19 and 20 depend from and further restrict claim 18, and claim 25 depends from and further restricts claim 24. These claims are also not anticipated by Heisch, at least by virtue of their dependency.

Therefore, the rejection of claims 1-5 and 8-25 under 35 U.S.C. § 102 has been overcome.

Furthermore, Heisch does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Heisch actually teaches away from the presently claimed invention because it teaches a comparing an address of an instruction to be executed with an address stored in an IABR as opposed to a performance indicator that identifies that execution of the instruction is to be monitored is present as in the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to implement Heisch to include a performance indicator that identifies that execution of the instruction is to be monitored is present as in the presently claimed invention, one of ordinary skill in the art would not be led to modify Heisch to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Heisch in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

III. 35 U.S.C. § 102, Anticipation – Claims 1, 6 and 7

The Examiner has rejected claims 1, 6 and 7 under 35 U.S.C. § 102(b) as being anticipated by Short (Short, K.L. "Embedded Microprocessor Systems Design: An Introduction Using the Intel 188EB", Prentice-Hall, Inc: 1998, Page 761). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> As per claim 1, Short discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether an indicator is associated with the instruction; and forcing an interrupt if the indicator is associated with the instruction. *The examiner asserts that if the opcode of the instruction (indicator) indicates the Interrupt instruction (Short pg. 761), an interrupt will be forced.*

Office Action dated January 27, 2006, page 10.

Short appears to describe activation of an interrupt procedure specified by an interrupt-type operand. Short does not disclose or suggest "responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present", and also does not disclose or suggest "forcing an interrupt if the performance indicator is present" as recited in amended claim 1. Short accordingly, does not anticipate claim 1 and claim 1 patentably distinguishes over Short in its present form.

Claims 6 and 7 depend from and further restrict claim 1, and are also not anticipated by Short, at least by virtue of their dependency.

Therfore, the rejection of claims 1, 6 and 7 under 35 U.S.C. § 102(b) has been overcome.

IV. Conclusion

For all the above reasons, it is respectfully urged that claims 1-25 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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